EXPRESS MAIL LABEL NO. EL902321413US

PD990053

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Edgar Wursthorn

Filed : Herewith

For : PHASE DETECTOR FOR A PHASE-LOCKED LOOP

PRELIMINARY AMENDMENT

Hon. Commissioner of Patents and Trademarks
Box PCT
Washington, D.C. 20231

Sir:

In the US national phase application of PCT/EP00/08064 filed herewith, please enter the following amendments:

IN THE SPECIFICATION:

Please amend the specification as follows:

On Page 1, line 2, please insert the following paragraph:

-- This application claims the benefit, under 35 U.S.C. § 365 of International Application PCT/EP00/08064, filed August 18, 2000, which was published in accordance with PCT Article 21(2) on March 8, 2001 in English and which claims the benefit of German patent application No. 19941445.9 filed August 30, 1999.--

IN THE CLAIMS:

Please amend the claims (which are the annexes of the International Preliminary Examination Report) as follows. A marked-up version of the claims is attached hereto:

1.(AMENDED) Phase detector for a phase-locked loop for digital input signals in which the digital summed value for a particular number of bits is equivalent to Zero, said phase detector having a sampled and digitized data signal supplied to it, having a delay stage for delaying the data signal by one or more sampling clock periods, having a subtraction stage, to which the undelayed and the delayed data signal are supplied, and comprising a filter or control stage to which the output of the subtraction stage are supplied at whose output the phase error can be tapped off, wherein a processing stage is provided, located between the subtraction stage and the filter or control stage, which assigns one of a plurality of possible output values, to the respective differential value, wherein the full differential value range is subdivided in a number of sub-ranges corresponding to the plurality of possible values, so that all differential values in one of the sub-ranges will get the same output value assigned.

3.(AMENDED) Phase detector according to Claim 1, wherein said control stage is a PI controller.

4.(AMENDED) Phase detector according to Claim 1, in which the delayed digital sample is deducted from the undelayed digital sample in the subtraction stage in each case.

5.(AMENDED) Phase detector according to Claim 1, in which a rectifier for signal conditioning is provided which has the sampled and digitized data signal supplied to it, the data signal being a ternary data signal, in particular.

6.(AMENDED) Phase detector according to Claim 5, in which the sampled and digitized ternary data signal is supplied, before rectification, to a separating stage in which the data signal is separated into a positive and a negative path.

7.(AMENDED) Phase detector according to Claim 6, in which separate delay, subtraction and processing stages or delay and comparison stages are provided for each path, and in which an addition stage is provided in which the assigned output values from the processing or comparison stages are added and, combined in this way, are passed on to the filter or control stage.

8.(AMENDED) Phase detector according to Claim 7, in which, in addition to the separate delay, subtraction and processing stages or delay and comparison stages for the positive and the negative path, there are also separate delay, subtraction and processing stages or delay and comparison stages for a further path, in which the complete data signal, including the positive and the negative path, is processed, the output values assigned by the processing stages or comparison stages likewise being supplied to the addition stage.

9.(AMENDED) Use of the phase detector according to Claim 1 in a phase-locked loop to recover the data clock signal for a digital signal.

IN THE ABSTRACT:

Please add the following Abstract.

-- The invention proposes a phase detector for a phase-locked loop. In this context, it relates to an improvement in the phase detector which can be used in a digital PLL circuit. The invention consists in a sampled and digitized data signal being supplied to the phase detector as an input signal. This data signal is delayed by a sampling clock signal in a delay stage. The delayed data signal and the undelayed data signal are then supplied to a subtraction stage. The difference between the two input values is formed in

this subtraction stage. The differential value determined is then analysed in a processing stage and one of a plurality of possible values is assigned to it. This is done on the basis of the value range in which the differential value is situated. The assigned value is then passed on as an output value to a filter/control stage, at whose output a phase error can then be tapped off. The solution described can be integrated very easily on a chip and affords a very advantageous response for the PLL control. --

REMARKS

The specification has been amended to include a reference to the priority applications.

Claims 1, and 3-9 have been amended to remove reference indicia and multiple dependencies and to meet the requirements of the United States. Claims 2 and 10 remain unchanged.

To meet the requirements of the United States, the Abstract (as originally filed in the PCT application) is added.

No fee is believed to have been incurred by virtue of this amendment. However if a fee is incurred on the basis of this amendment, please charge such fee against deposit account 07-0832

Respectfully submitted,
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February 13, 2002

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MARKED UP VERSION OF THE AMENDED SPECIFICATION

On Page 1, line 2, please insert the following paragraph:

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MARKED UP VERSION OF THE AMENDED CLAIMS

1.(AMENDED) Phase detector for a phase-locked loop for digital input signals in which the digital summed value for a particular number of bits is equivalent to Zero, said phase detector having a sampled and digitized data signal supplied to it, having a delay stage [(52)] for delaying the data signal by one or more sampling clock periods, having a subtraction stage [(53)], to which the undelayed and the delayed data signal are supplied, and comprising a filter or control stage [(60)], to which the output of the subtraction stage [(53)] are supplied at whose output the phase error can be tapped off, [characterized in that] wherein a processing stage [(54)] is provided, located between the subtraction stage and the filter or control stage [(60)], which assigns one of a plurality of possible output values, to the respective differential value, wherein the full differential value range is subdivided in a number of sub-ranges corresponding to the plurality of possible values, so that all differential values in one of the sub-ranges will get the same output value assigned.

3.(AMENDED) Phase detector according to Claim 1 [or 2], wherein said control stage [(60)] is a PI controller.

4.(AMENDED) Phase detector according to [one of Claims 1 to 3] Claim 1, in which the delayed digital sample is deducted from the undelayed digital sample in the subtraction stage [(53)] in each case.

5.(AMENDED) Phase detector according to [one of Claims 1 to 4] Claim 1, in which a rectifier [(51)] for signal conditioning is provided which has the sampled and digitized data signal supplied to it, the data signal being a ternary data signal, in particular.

6.(AMENDED) Phase detector according to Claim 5, in which the sampled and digitized ternary data signal is supplied, before rectification, to a separating stage [(55)] in which the data signal is separated into a positive and a negative path.

7.(AMENDED) Phase detector according to Claim 6, in which separate delay, subtraction and processing stages [(52, 53, 54)] or delay [(52)] and comparison stages are provided for each path, and in which an addition stage [(56)] is provided in which the assigned output values from the processing [(54)] or comparison stages are added and, combined in this way, are passed on to the filter or control stage [(60)].

8.(AMENDED) Phase detector according to Claim 7, in which, in addition to the separate delay, subtraction and processing stages [(52, 53, 54)] or delay [(52)] and comparison stages for the positive and the negative path, there are also separate delay, subtraction and processing stages [(52, 53, 54)] or delay [(52)] and comparison stages for a further path, in which the complete data signal, including the positive and the negative path, is processed, the output values assigned by the processing stages [(54)] or comparison stages likewise being supplied to the addition stage [(56)].

9.(AMENDED) Use of the phase detector according to [one of Claims 1 to 8] Claim 1 in a phase-locked loop to recover the data clock signal for a digital signal.